RAISONI GROUP
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G. H. Raisoni College of Engineering & Management,

Wagholi, Pune.

(Autonomous Institute)

Department of Electronics & Telecommunication

Post Graduate Course

HAND BOOK

M TECH (VLSI & EMBEDDED SYSTEMS)

Academic Year 2016-17

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VISION AND MISSION OF G.H.RAISONI COLLEGE OF ENGINEERING AND MANAGEMENT

VISION:-

To achieve excellent standards of quality education by keeping pace with rapidly changing technologies.

To create technical manpower of global standards with capabilities of accepting new challenges.

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MISSION:-

Our efforts will be dedicated to impart quality and value based education to raise satisfaction level of all stake-holders.Our strength will be directed to create competent engineers.

Our endeavor will be to provide all support to promote research& development activities.

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VISION AND MISSION TheDepartment of

Electronics &Telecommunication Engineering

Vision

"To create competent engineers in electronics and telecommunication engineering, employable in global market."

Mission

" Our emphasis will be directed to work synergistically to step towards quality education & technical knowledge to enhance technical skills & ethical values for global employment."

Programme Educational Objectives (PEOs)

- To make ourstudentssuccessfulElectronics and Telecommunication Engineering Gradu[illegible]

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- To train students with strong fundamental knowledge in mathematics, science and Electronics and Telecommunication Engineering to pursue higher education, to remain productive and to develop research approach.
- To develop and apply hardware and software skill to analyze, design and create electronic products and provide solutions to solve engineering problems.
- To provide experimental experience to understand theoretical andpractical aspects of engineering.
- To enable students to get employment in electronics, communication, information technology and in other disciplines too.
- To inculcate communication skills, leadership qualities, ethical attitude and teamwork spirit needed while working in professionaldynamicnational and multinational organizations.

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Programme Outcomes (POs)

1 An ability to analyse, design, and implement hardware and software computer systems as well as control systems, communications systems, embedded systems or instrumentation systems.

2 An ability to apply knowledge of mathematics, science, engineering, and technology to engineering problems.

3 An ability to design and conduct standard tests and measurements, and to analyse, interprets experiments and report results.

4 An ability to demonstrate skills to use modern engineering tools, software and equipment to analyse and finding solution to the engineering problems.

5 An ability to work in laboratory having multidisciplinary tasks.

6 An ability to understand electronics circuits and its analysis.

7 An ability to develop application of electric circuits, computer programming associated software applications, analog and digital electronics, microcomputers, operating systems.

8 An ability to communicate effectively.

9 Graduate will develop confidence for self-education and ability for life-long learning through higher education.

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10 An ability to understand professional and ethical responsibility.

11 An ability to function effectively as a member or leader in a technical team

List of PSOs	
1	Design of complex VLSI/ES based electronic systems
2	Development of software program for complex system
3	Writing of technical Journal Paper, research publication
4	Acquire effective verbal communication & interpersonal skills

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EXPERTS WHO DESIGNED SCHEME & SYLLABUS

Electronics and Telecommunication Engineering

SN	Name	Designation	Designation in BoS
1	Dr. TanujaDhope	Associate Professor,HOD E&TC	**Chairman**
2	Dr. Preeti Bajaj	Director, GHRCE, Nagpur	**Special Invitee**
3	Dr. R. S. Bichkar	Incharge Director, GHRCEM and Professor, UG-E&TC	**Permanent Invitee**
4	Mr. P. N. Matte	Assistant Professor UG-E&TC & Vice Principal (Academics)	**Faculty Representative** (Specialized faculty in VLSI Design, Embedded Syste Design.)
5	Dr. ParulArora	Assistant Professor UG-E&TC	**Faculty Representative** **(**Specialized faculty in Image Processing Signal Processing)
6	Dr. M.S. Sutaone	Professor (E&TC), College of Engineering, Pune	**Subject Expert** (Specialized faculty in VLSI Design, Signal & Image Processing)
7	Dr. V.M. Gadre	Professor, IIT, Bombay	**Subject Expert** (Specialized faculty in Digital Signal Processing)
8			**Subject Expert to be**

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			nominated by Vice Chancellor
9	Mr. Sanjay Mishra	Vice President Cotmac Electronics Pvt. Ltd.	**Industry Expert**
10	Mr. Prasanna Rode	Principal, Architect, Capgemini	**Industry Expert**
11	Mr. Anuj Sharma	Engineer (R&D), KPIT Cummins Info Systems Ltd., Pune	**Alumni Member**
12	Mr. RajshekharSanda	UG Student	**Student Member- UG**
13	Ms. SupriyaGaikwad	PG Student	**Student Member- PG**
14	Prof. Vijaykumar Joshi	Professor & Head, PG-E&TC	**Co-opted Member** **(Specialized Faculty in Communication Engg.)**
15	Mr. S. K. Waghmare	Assistant Professor & Head, Incubation Center and Innovation Cell	**Co-opted Member** **(Specialized Faculty in VLSI & RFM EMS)**
16	Ms. RupaliB.Patil	Assistant Professor UG-E&TC	**Co-opted Member** **(Specialized Faculty in Communication Engg.)**
17	DrMilindKhanapurkar	Professor, HOD E&TC GHRCE, Nagpur	**Co-opted Member**

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M Tech. VLSI & Embedded System

Course Code Details

S. N.	Code	Course Name	Sem	Scheme	Sub	Elective	Offer
1	MVEL501	Digital CMOS Design	I	VLSI & Embedded System 2016-17 (AUTONOMOUS)	Theory	NO	YES
2	MVEL502	Embedded System Design	I	VLSI & Embedded System 2016-17 (AUTONOMOUS)	Theory	NO	YES
3	MVEL503	Reconfigurable Computing	I	VLSI & Embedded System 2016-17 (AUTONOMOUS)	Theory	NO	YES
4	MVEL504	Research Methodology	I	VLSI & Embedded System 2016-17 (AUTONOMOUS)	Theory	NO	YES
5	MVEL505	Elective I	I	VLSI & Embedded System 2016-17 (AUTONOMOUS)	Theory	YES	YES
6	MVEP506	Lab I	I	VLSI & Embedded System 2016-17 (AUTONOMOUS)	Practical	NO	YES
7	MVESD501	Advanced Skill Development	I	VLSI & Embedded System 2016-17 (AUTONOMOUS)	Practical	NO	YES
8	MVEL507	Analog CMOS Design	II	VLSI & Embedded System 2016-17 (AUTONOMOUS)	Theory	NO	YES
9	MVEL508	System on	II	VLSI & Embedded System 2016-17	Theory	NO	YES

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		Chip		(AUTONOMOUS)			
10	MVEL509	Processor Design	II	VLSI & Embedded System 2016-17 (AUTONOMOUS)	Theory	NO	YES
11	MVEL510	Elective II	II	VLSI & Embedded System 2016-17 (AUTONOMOUS)	Theory	YES	YES
12	MVEL511	Elective III	II	VLSI & Embedded System 2016-17 (AUTONOMOUS)	Theory	YES	YES
13	MVEP512	Lab Practice II	II	VLSI & Embedded System 2016-17 (AUTONOMOUS)	Practical	NO	YES
14	MVEP513	Seminar I	II	VLSI & Embedded System 2016-17 (AUTONOMOUS)	Seminar	NO	YES
15	MVESD601	Technical Writing (LATEX)	III	VLSI & Embedded System 2016-17 (AUTONOMOUS)	Practical	NO	YES
16	MVEP602	Seminar-II	III	VLSI & Embedded System 2016-17 (AUTONOMOUS)	Seminar	NO	YES
17	MVEP603	Dissertation Phase I	III	VLSI & Embedded System 2016-17 (AUTONOMOUS)	Dissertation	NO	YES
18	MVEP604	Seminar - III	IV	VLSI & Embedded System 2016-17 (AUTONOMOUS)	Seminar	NO	YES
19	MVEP605	Dissertation Phase II	IV	VLSI & Embedded System 2016-17 (AUTONOMOUS)	Dissertation	NO	YES

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M Tech. VLSI & Embedded System

Course Structure

Scheme of Examination for M.Tech E&TC (VLSI & Embedded System) Course												
Branch- E&TC												
Semester- I												
Subject code	**Subject Name**	**Teaching scheme (Weekly Load in Hrs)**				**Credits**	**Evaluation Scheme**					**ESE Duration (Hrs)**
							Theory			**Practical**	**Total**	
		Lecture	**Tutorial**	**Practical**	**Total**		**TAE 20%**	**CAE 20%**	**ESE 60%**	**(Cont. Ass.)**		
MVEL501	Digital CMOS Design	3	1	_	4	4	20	20	60	_	100	3
MVEL502	Embedded System Design	3	1	_	4	4	20	20	60	_	100	3
MVEL503	Reconfigurable Computing	3	1	_	4	4	20	20	60	_	100	3
MVEL504	Research Methodology	3	-	_	3	3	20	20	60	_	100	3
MVEL505	Elective I	3	-	_	3	3	20	20	60	_	100	3
MVEP506	Lab I	_	_	4	4	2	_	_	_	100	100	_
MVESD501	Advanced Skill Development			2	2	AU				-		
	Total	15	3	6	24	20	100	100	300		600	
Elective-I MVEL505												
MVEL505A. Real Time Operating System												
MVEL505B. Mixed Signal Circuit Design												

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MVEL505C. CMOS RF Circuit Design
MVEL505D. Wireless sensor Network

Scheme of Examination for M.Tech E&TC (VLSI & Embedded System) Course												
Branch- E&TC												
Semester- II												
Subject code	**Subject Name**	**Teaching scheme (Weekly Load in hrs)**				**Credits**	**Evaluation Scheme**					
							Theory			**Practical**	**Total**	
		Lecture	**Tutorial**	**Practical**	**Total**		**TAE 20%**	**CAE 20%**	**ESE 60%**	**(Con.Ass.+ External)**		
MVEL507	Analog CMOS Design	3	1	_	4	4	20	20	60	_ _	100	
MVEL508	System on Chip	3	1	_	4	4	20	20	60	_ _	100	
MVEL509	Processor Design	3		_	3	3	20	20	60	_ _	100	
MVEL510	Elective II	3	_	_	3	3	20	20	60	_	100	
MVEL511	Elective III	3			3	3	20	20	60		100	
MVEP512	Lab Practice II	_	_	4	4	2	_	_	_	100	100	
MVEP513	Seminar I			2	2	2				100	100	
Total		15	2	6	21	21	100	100	300	200	700	

Elective-III (MVEL511)	**Elective - II MVEL510**
MVEL511A. ASIC Design	**MVEL510A**.Microelectronic microwave switches Design(MEMS)
MVEL511B. Network on Chip	
MVEL511C.DSP Processor & Architectures	**MVEL510B**. VLSI Interconnection

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MVEL511D. Software Defined Radio	**MVEL510C.** Embedded Product Design
MVEL511E. Energy Studies	**MVEL510D**. Optimization Technique
MVEL511F. Environmental Studies	**MVEL510E**. Design and Analysis of Algorithm
MVEL511G. Open Elective	**MVEL510F**. Industry Offered Elective

Scheme of Examination for M. Tech. E & TC Engineering													
VLSI Embedded System Course													
Semester- III													
Subject code	**Subject Name**	**Teaching scheme (Weekly Load in hrs.)**				**Credits**	**Evaluation Scheme**						**ESE Duration (Hrs.)**
							Theory			**PR**		**Total**	
		Lecture	**Tutorial**	**Practical**	**Total**		**TAE 20 %**	**CAE 20 %**	**ESE 60%**	**Internal**	**External**		
MVESD601	Technical Writing (LATEX)	-	-	2	2	2	-	-	-	50	50	100	_
MVEP602	Seminar-II	-	-	4	4	4	-	-	-	50	50	100	-
MVEP603	Dissertation Phase I	-	-	8	8	8	-	-	-	150	50	200	-
	Total	-	-	14	14	14	-	-	-	250	150	400	-

Scheme of Examination for M. Tech. E & TC Engineering													
VLSI Embedded System Course													
Semester-IV													
Subject code	**Subject Name**	**Teaching scheme (Weekly Load in hrs.)**				**Credits**	**Evaluation Scheme**						**ESE Duration (Hrs.)**
							Theory			**PR**		**Total**	
		Lecture	**Tutorial**	**Practical**	**Total**		**TAE 20 %**	**CA E 20 %**	**ESE 60%**	**Internal**	**External**		

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MVEP604	Seminar - III	-	-	4	4	4	-	-	-	50	50	100	-
MVEP605	Dissertation Phase II	-	-	16	16	16	-	-	-	150	50	200	-
	Total	-	-	20	20	20	-	-	-	200	100	300	-

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Detailed Syllabus

Scheme of Examination for M.Tech E&TC (VLSI & Embedded System) Course												
Branch- E&TC												
Semester- I												
Subject code	**Subject Name**	**Teaching scheme (Weekly Load in Hrs)**				**Credits**	**Evaluation Scheme**					**ESE Duration (Hrs)**
							Theory			**Practical**	**Total**	
		Lecture	**Tutorial**	**Practical**	**Total**		**TAE 20%**	**CAE 20%**	**ESE 60%**	**(Cont. Ass.)**		
MVEL501	Digital CMOS Design	3	1	_	4	4	20	20	60	_	100	3
MVEL502	Embedded System Design	3	1	_	4	4	20	20	60	_	100	3
MVEL503	Reconfigurable Computing	3	1	_	4	4	20	20	60	_	100	3
MVEL504	Research Methodology	3	-	_	3	3	20	20	60	_	100	3
MVEL505	Elective I	3	-	_	3	3	20	20	60	_	100	3
MVEP506	Lab I	_	_	4	4	2	_	_	_	100	100	_
MVESD501	Advanced Skill Development			2	2	AU				-		
	Total	15	3	6	24	20	100	100	300		600	
Elective-I MVEL505												
MVEL505A. Real Time Operating System												
MVEL505B. Mixed Signal Circuit Design												

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MVEL505C. CMOS RF Circuit Design
MVEL505D. Wireless sensor Network

MVEL501: DIGITAL CMOS DESIGN		
Teaching Scheme:	**Examination Scheme (Theory)**	**Examination Scheme(Laboratory)**
Lectures: 3 Hrs/Week **Tutorials:** 1 Hr/Week **Practical:** Nil	**TAE:** 20 Marks **CAE :** 20 Marks **ESE : 6**0 Marks	**Practical:** Nil
Credit	**4**	
Prerequisite(If any): Nil		
Course Outcome:		
1. The student will understand the fundamentals of CMOS Technology in Digital Domain.		
2. The student will show the skills of designing digital VLSI.		
3. The student will demonstrate the ability for using backend tools in IC technology.		

Course Contents	**Hrs**
Unit – I :Module I	8
MOSFET Models and Layout: MOS Capacitance models, MOS Gate Capacitance Model, MOS Diffusion Capacitance Model. Non ideal I-V Effects, MOSFET equivalent circuits and analysis, Parasitic; Technology scaling; Lambda parameter; wiring parasitic; SPICE Models, CMOS layout techniques; Transient response. CMOS Technologies: Layout Design Rules CMOS Process Enhancements: Transistors, Interconnect, Circuit Elements, Beyond Conventional CMOS. CMOS Fabrication and Layout: Inverter Cross-section, Fabrication Process, Stick Diagrams.	
Unit – II : Module II	8
Performance parameters Static, dynamic and short circuit power dissipations; Propagation delay; Power delay product; Fan in, fan out and dependencies. Delay Estimation: RC Delay	

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Models, Linear Delay Model, Logical Effort, Parasitic Delay. Logical Effort and Transistor Sizing: Delay in a Logic Gate, Delay in Multistage Logic Networks, Interconnect: Resistance, Capacitance, Delay, Crosstalk. Design Margin:	
Unit – III : Module III	8
Logic design Static CMOS Logic : Inverter, NAND Gate, Combinational Logic, NOR Gate, Compound Gates, Pass Transistors and Transmission Gates, Tractates, Multiplexers, Latches and Flip-Flops, Design calculations for combinational logic and active area on chip; Hazards, sources and mitigation techniques, case study; HDL codes for FSM, Met stability and solutions; Transmission gate, utility and limitations	
Unit – IV : Module IV	
Advanced trends Circuit Families: Static CMOS, Rationed Circuits, Cascade Voltage Switch Logic, Dynamic Circuits, Domino logic; NORA logic, Differential Circuits, Sense Amplifier Circuits, BiCMOS Circuits, Low Power Logic Design, Comparison of Circuit Families, Materials for performance improvement, Techniques for Low power, high speed designs	8

Text Books: (Book Title, Name of the author, name of the Publisher, edition, year of publication)
1. Neil Weste and Kamaran, “Principles of CMOS VLSI Design”, Education Asia.
2. J. M. Rabaey, A. Chandrakasan and B. Nikolic, Digital Integrated Circuits : A Design Perspective, Pearson (Low Price Edition)
Reference Books:
1. Neil Weste and Kamaran, “Principles of CMOS VLSI Design”, Education Asia.
2. J. M. Rabaey, A. Chandrakasan and B. Nikolic, Digital Integrated Circuits : A Design 3. Perspective, Pearson (Low Price Edition)
4. Charles Roth, “Digital System Design using VHDL”, Tata McGraw Hill.
5. S-M. Kang and Y. Leblebici, CMOS Digital Integrated Circuits : Analysis and Design, Third Edition, McGraw-Hill

MVEL502: EMBEDDED SYSTEM DESIGN		
Teaching Scheme:	**Examination Scheme (Theory)**	**Examination Scheme (Laboratory)**
Lectures:3 Hrs/Week **Tutorials:** 1Hr/Week **Practical:**Nil	**TAE:**20 Marks **CAE :**20 Marks**ESE:**60 Marks	**Practical:**Nil

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Credit	4	

Course Objective:

1. Understanding use of microcontroller in embedded systems.
2. Understanding & practicing design issue related to Microcontroller based Embedded System design.
3. Understanding & practicing of programming by use of advanced tools.

Course Outcome:

1. The student will study ARM Processor based Embedded System design
2. The student will be able to do programming in Embedded programming in C, C++
3. The student will understand Linux operating system and device driver
4. The student will demonstrate the knowledge of android operating system

Course Contents	Hrs
Unit – I : Module I	8
Introduction to Embedded Systems Introduction to Embedded Systems, Architecture of Embedded System, Design Methodology, Design Metrics, General Purpose Processor, System On chip. **Embedded system design and development:** Embedded system design**,** Life-Cycle Models, Problem solving, The design process, Requirement identification, Formulation of requirements specification. Development tools . **System design specifications:** System specifications versus system requirements, Partitioning and decomposing a system, Functional design, Architectural design, Functional model versus architectural model, Prototyping, Other considerations, Archiving the project.	
Unit – II : Module II	8
ARM-9 Architecture: ARM-9-TDMI Processor core, ARM architectural support for high level language, ARM architectural support for system development, ARM architectural support for operating System, Memory subsystem architecture, Designing a cache system, Memory allocation, Communication protocols.	
Unit – III : Module III	8
Embedded Linux: System architecture, BIOS versus boot-loader, Booting the kernel, Kernel initialization, Space initialization, Boot loaders, Storage considerations **Linux kernel construction**: Kernel build system, Obtaining a custom Linux kernel, File systems, Device drivers,Kernel configuration.	
Unit – IV : Module IV	8
Android Operating System Introduction to Android technology, Structure of Android applications, Understanding Manifest, Working with Activities, Data stores, Network services and APIs, Intents, Content Providers and services, Advance Operations with Android, Telephony and SMS, Audio Video using the Camera, Project Discussion on Android.	

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Text Books: (Book Title, Name of the author, name of the Publisher, edition, year of publication)
1. Steve Ferber, “ARM System-on-Chip Architecture”, Second Edition, Pearson Education Publication
2. James K. Peckol, “Embedded Systems: A Contemporary Design Tool”, WILEY Student Edition Publication
Reference Books:
1. Steve Furber, “ARM System-on-Chip Architecture”, Second Edition, Pearson Education Publication
2. James K. Peckol, “Embedded Systems: A Contemporary Design Tool”, WILEY Student Edition Publication
3. TmmyNoergaard, “Embedded Systems Architecture”, Elsevier Publication
4. CristopherHallinan, “Embedded Linux Primer: A Practical Real-World Approach”, Second Edition, Pearson Education Publication
5. CaigHollabaugh, “Embedded Linux, Hardware, Software and Interfacing”, Pearson Education Publication

MVEL503: RECONFIGURABLE COMPUTING		
Teaching Scheme:	**Examination Scheme (Theory)**	**Examination Scheme (Laboratory)**
Lectures:3 Hrs/Week **Tutorials:** 1Hr/Week **Practical:**Nil	**TAE:**20 Marks **CAE :**20 Marks**ESE: 6**0 Marks	**Practical:**Nil
Credit	**4**	
Course Objective:		
1. To understand the concepts of architecture reconfigurability, programmable logic devices and optimization of the Reconfigurable computer architecture to the task algorithm and data structure.		
2. To understand the basics of the Complex Programmable Logic Devices (CPLD) and Field Programmable Gate Array (FPGA) organization and Reconfigurable computer architectures based on these devices.		
3. To understand and identify Reconfigurable Computing Systems (RCS) application in DSP, Video/Image Processing and Supercomputing applications		
Course Outcome:		
1. The student will understand concept of static and dynamic reconfiguration.		
2. The student will use the basics of the PLDs for designing reconfigurable circuits.		
3. The student will understand the reconfigurable system design using HDL		
Course Contents		**Hrs**
Unit – I : Module I		8
Types of computing and introduction to RC: General Purpose Computing, Domain-Specific Processors,		

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Application Specific Processors; Reconfigurable Computing, Fields of Application; Reconfigurable Device Characteristics, Configurable, Programmable, and Fixed-Function Devices; General-Purpose Computing, General-Purpose Computing Issues;	
Unit – II : Module II	8
Metrics: Density, Diversity, and Capacity; Interconnects, Requirements, Delays in VLSI Structures; Partitioning and Placement, Routing; Computing Elements, LUTs, LUT Mapping,ALU and CLBs; Retiming, Fine-grained & Coarse-grained structures; Multi-context**;**	
Unit – III : Module III	8
Different architectures for fast computing viz. PDSPs, RALU, VLIW, Vector Processors, Memories, CPLDs, FPGAs, Multi-context FPGA, Partial Reconfigurable Devices; Structure and Composition of Reconfigurable Computing Devices: Interconnect, Instructions, Contexts, Context switching, RP space model;	
Unit – IV : Module IV	8
Reconfigurable devices for Rapid prototyping, Non-frequently reconfigurable systems, Frequently reconfigurable systems; Compile-time reconfiguration, Run-time reconfiguration; Architectures for Reconfigurable computing: TSFPGA, DPGA, Matrix; Applications of reconfigurable computing: Various hardware implementations of Pattern Matching such as the Sliding Windows Approach, Automaton-Based Text Searching. Video Streaming;	

Text Books: (Book Title, Name of the author, name of the Publisher, edition, year of publication)
1. Andre Dehon, “Reconfigurable Architectures for General Purpose Computing”.
2. IEEE Journal papers on Reconfigurable Architectures.
Reference Books:
1. Andre Dehon, “Reconfigurable Architectures for General Purpose Computing”.
2. IEEE Journal papers on Reconfigurable Architectures.
3. “High Performance Computing Architectures” (HPCA) Society papers.
4. Christophe Bobda, “Introduction to Reconfigurable Computing”, Springer Publication.
5. MayaGokhale, Paul Graham, “Reconfigurable Computing”, Springer Publication.

MVEL504 : RESEARCH METHODOLOGY		
Teaching Scheme:	**Examination Scheme (Theory)**	**Examination Scheme(Laboratory)**

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Lectures:3 Hrs/Week **Tutorials:** 1Hr/Week **Practical:**Nil	**TAE:**20 Marks **CAE :**20 Marks**ESE: 6**0 Marks	**Practical:**Nil
Credit	**3**	

Prerequisite (If any): Nil

Course Objective:

1. To gain insights into how scientific research is conducted.
2. To help in critical review of literature and assessing the research trends, quality and extension potential of research and equip students to undertake research.
3. To learn and understand the basic statistics involved in data presentation.
4. To identify the influencing factor or determinants of research parameters.
5. To test the significance, validity and reliability of the research results.
6. 6. To help in documentation of research results.

Course Outcome:

1. The student will learn research problem & its scope, objectives, and errors.
2. The student will learn the basic instrumentation schemes & data collection methods.
3. The student will study the various statistical techniques.
4. The students will study modeling and predict the performance of experimental system.
5. The student will learn to develop the research proposals.

Course Contents	**Hrs**
Unit – I :Module I	8
Research Problem: Meaning of research problem, Sources of research problem, Criteria/Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. **Basic instrumentation:**Instrumentation schemes, Static and dynamic characteristics of instruments used in experimental set up, Performance under flow or motion conditions, Data collection using a digital computer system, Linear scaling for receiver and fidelity of instrument, Role of DSP is collected data contains noise.	
Unit – II : Module II	8
Applied statistics Regression analysis, Parameter estimation, Multivariate statistics, Principal component analysis Moments and response curve methods, State vector machines and uncertainty analysis.	
Unit – III : **Module III**	8
Modeling and prediction of performance Setting up a computing model to predict performance of experimental system, Multiscalemodeling and verifying performance of process system, Nonlinear analysis of system and asymptotic analysis, Verifying if assumptions hold true for a given apparatus setup, Plotting family of performance curves to study trends	

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and tendencies, Sensitivity theory and applications	
Unit – IV : Module IV	8
Developing a Research Proposal Format of research proposal, Individual research proposal, Institutional proposal. Proposal of a student– a presentation and assessment by a review committee consisting of Guide and external expert only. Other faculty members may attend and give suggestions relevant to topic of research.	

Text Books: (Book Title, Name of the author, name of the Publisher, edition, year of publication)
1. Research methodology: an introduction for science & engineering students", by Stuart Melville and Wayne Goddard
2. Research Methodology: An Introduction" by Wayne Goddard and Stuart Melville
Reference Books:
1. Research methodology: an introduction for science & engineering students", by Stuart Melville and Wayne Goddard
2. „Research Methodology: An Introduction" by Wayne Goddard and Stuart Melville
3. Research Methodology: A Step by Step Guide for Beginners", by Ranjit Kumar, 2nd Edition
4. „Research Methodology: Methods and Trends", by Dr. C. R. Kothari
5. Operational Research" by Dr. S.D. Sharma, KedarNath Ram Nath& co.

Elective-I

MVEL505A: REAL-TIME OPERATING SYSTEMS		
Teaching Scheme:	**Examination Scheme (Theory)**	**Examination Scheme (Laboratory)**
Lectures:3 Hrs/Week **Tutorials:** 1Hr/Week **Practical:**Nil	**TAE:**20 Marks **CAE :**20 Marks**ESE:**60 Marks	**Practical:**Nil
Credit :	**3**	
Course Objective:		

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1. Ability to apply knowledge of RTOS based design.	
2. To solve problems and introduce device and buses for embedded networking.	
3. Explain Real time operating system for inter & intra task communication models	
Course Outcome:	
1. Describe the general architecture of computers.	
2. Describe, contrast and compare differing structures for operating systems	
3. Understand and analyses theory and implementation of: processes, resource control (concurrency etc.),physical and virtual memory, scheduling, I/O and files	
Course Contents	**Hrs**
Unit – I : Basic Principles - Operating System structures – System Calls – Files – Processes – Design and Implementation of processes – Communication between processes –Introduction to Distributed operating system – Distributed scheduling	8
Unit – II : RTOS Task and Task state - Process Synchronization- Message queues – Mail boxes – pipes Critical section – Semaphores – Classical synchronization problem – Deadlocks	8
Unit – III : Event Based – Process Based and Graph based Models – Real Time Languages – RTOS Tasks – RT scheduling - Interrupt processing – Synchronization – Control Blocks –Memory Requirements.	8
Unit – IV : Principles – Design issues – Polled Loop Systems – RTOS Porting to a Target –Comparison and study of various RTOS like QNX – VX works – PSOS – C Executive –Case studies.	8
Unit – V : RTOS for Image Processing – Embedded RTOS for voice over IP – RTOS for fault Tolerant Applications – RTOS for Control Systems.	8

Text Books: (Book Title, Name of the author, name of the Publisher, edition, year of publication)
1. Real-Time Systems Jane W.S. Liu Prentice Hall. 2002 1st
2. Operating Systems Principle Peter Galvin and Abraham SilberschatzPenramInternational& Thomson Asia 2004 2nd
Reference Books:
1. Real-Time Systems Jane W.S. Liu Prentice Hall. 2002 1st
2. Operating Systems Principle Peter Galvin and Abraham SilberschatzPenramInternational& Thomson Asia 2004 2nd
3. Embedded Systems Architecture programming and Design Raj kamalMcGraw-Hill Publishing Company 2002 1st
4. Real – Time Systems and software Alan C. Shaw John Wiley & Sons Inc 2001 1st

MVEL505B : MIXED SIGNAL CIRCUIT DESIGN		
Teaching Scheme:	**Examination Scheme (Theory)**	**Examination Scheme (Laboratory)**

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Lectures:3 Hrs/Week **Tutorials:** 1Hr/Week **Practical:**Nil	**TAE:**20 Marks **CAE :**20 Marks**ESE:**60 Marks	**Practical:**Nil
Credit :	**3**	

Prerequisite (If any):

1. Analog VLSI

Course Objective:

1. This Mixed Signal processing course provides comprehensive techniques on the essential concepts of Mixed Signal Testing. This information is designed to elevate the baseline understanding and capabilities of product/test engineers.
2. This subject introduces digital test and linear test engineers to the mixed signal world by teaching the basics of analog and mixed signal test methods. Sampling Theory, Frequency Domain Testing, and Digital Signal Processing.
3. The course applies these fundamental concepts to different test methods and data validation for mixed signal parameters together with debugging, noise reduction and device interface techniques.

Course Outcome:

1. Students will be able to Design and verification of digital circuit using high level circuit description language
2. Students will be able to Integrate the analog and digital circuits blocks and verify the complete mixed-signal structure over process, voltage and temperature variations.
3. Students will be able to use advanced tools available for design and verification digital circuit

Course Contents	**Hrs**
Unit – I : CMOS comparators, switched capacitor circuits and filters.	8
Unit – II : Dynamics of PLL, phase detector, loop filters, charge pump PLLs.	8
Unit – III : Data converter fundamentals, specifications,	8
Unit – IV : Nyquist rate D/A and A/D converters-Over sampling converters, noise shaping modulators,	8
Unit – V :multibite delta sigma converters	8

Text Books: (Book Title, Name of the author, name of the Publisher, edition, year of publication)

1. CMOS: Mixed-Signal Circuit Design R. Jacob Baker Wiley-Inter Sciences.1999 Second
2. CMOS Analog Circuit Design Allen and HolmbergDramatic Press 2001 1st

Reference Books:

1. CMOS: Mixed-Signal Circuit Design R. Jacob Baker Wiley-Inter Sciences.1999 Second
2. CMOS Analog Circuit Design Allen and HolmbergDreamtech Press 2001 1st
3. Design of Analog CMOS Integrated Circuits Razavi.by BPB Publication 2003 2nd

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MVEL505C: CMOS RF CIRCUIT DESIGN		
Teaching Scheme:	**Examination Scheme (Theory)**	**Examination Scheme (Laboratory)**
Lectures:3 Hrs/Week **Tutorials:** 1Hr/Week **Practical:**Nil	**TAE:**20 Marks **CAE :**20 Marks**ESE:**60 Marks	**Practical:**Nil
Credit :	**3**	

Prerequisite (If any):

1. VLSI Subsystem Design

Course Objective:

1. Introduce the theory and concept of radio frequency integrated system.
2. To analyze the performance parameters of radio frequency circuits and identify design trade-off of radiofrequency communication systems.
3. Students will perform practical design and simulation exercises using the electronic design automation tools
4. To enhance their understanding of the design problems encountered in comesrf integrated circuits.

Course Outcome:

1. Understanding of the design and analysis of radio frequency integrated circuits and systems (RFICs) for communications
2. Understanding the enabling integrated circuit technology and devices

Course Contents	**Hrs**
Unit – I : Characteristics of passive IC components at RF frequencies.	8
Unit – II : Two port noise theory, passive impedance transformation.	8
Unit – III : High frequency amplifier design, Low noise amplifiers.	8
Unit – IV : Mixers, RF power amplifiers.	8
Unit– V : Oscillators and synthesizers, phase noise considerations.	8

Text Books: (Book Title, Name of the author, name of the Publisher, edition, year of publication)

1. The Design of CMOS Radio-Frequency Integrated Circuits Thomas H. Lee Pearson 2002 2nd
2. Design of CMOS RF Integrated Circuits and Systems ManhAnh Do, ChirnChye Boon, KiatSengYeo TMH 2001 1st

Reference Books:

1. The Design of CMOS Radio-Frequency Integrated Circuits Thomas H. Lee Pearson 2002 2nd
2. Design of CMOS RF Integrated Circuits and Systems ManhAnh Do, ChirnChye Boon, KiatSengYeo TMH 2001 1st

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3. The Design of CMOS Radio- Frequency Integrated Circuits Thomas H. LeeCambridge University Press CMOS RFIC design Principles 1999 2nd

MVEL505D : WIRELESS SENSOR NETWORK		
Teaching Scheme:	**Examination Scheme (Theory)**	**Examination Scheme (Laboratory)**
Lectures:3 Hrs/Week **Tutorials:** 1Hr/Week **Practical:**Nil	**TAE:**20 Marks **CAE :**20 Marks**ESE:**60 Marks	**Practical:**Nil
Credit	**3**	
Prerequisite (If any):		
Course Objective:		
Course Outcome:		
1. The student will understand the architecture of WSN network.		
2. The student will understand the physical layer related aspects of WSN network.		
3. The student will exhibit the knowledge of power management in wireless communication systems.		
4. The student will exhibit the knowledge of security aspects of WSN systems.		

Course Contents	**Hrs**
Unit – I :Module I	8
Introduction : Motivation for a Network of Wireless Sensor Nodes , Sensing and Sensors Wireless Networks, Challenges and Constraints **Applications :** Health care, Agriculture, Traffic and others	
Unit – II : Module II	8
Architectures : Node Architecture; the sensing subsystem, processor subsystem, communication interface, LMote, XYZ, Hogthrob node architectures **Power Management** - Through local power, processor, communication subsystems and other means, time Synchronization need, challenges and solutions overview for ranging techniques. **Security** Fundamentals, challenges and attacks of Network Security, protocol mechanisms for security.	
Unit – III : Module III	8
Operating Systems -Functional and non functional Aspects, short overview of prototypes Tiny OS, SOS, Contiki, LiteOS, sensor grid.	
Unit – IV : **Module IV**	8
Physical Layer- Basic Components, Source Encoding, Channel Encoding, Modulation, Signal Propagation **Medium Access Control** – types, protocols, standards and characteristics, challenges **Network Layer** - Routing Metrics, different routing techniques	

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Text Books: (Book Title, Name of the author, name of the Publisher, edition, year of publication)
1. Dargie, W. and Poellabauer, C., "Fundamentals of wireless sensor networks: theory and practice", John Wiley and Sons, 2010
2. Sohraby, K., Minoli, D., Znati, T. "Wireless sensor networks: technology, protocols, and applications, John Wiley and Sons", 2007
Reference Books:
1. Dargie, W. and Poellabauer, C., "Fundamentals of wireless sensor networks: theory and practice", John Wiley and Sons, 2010
2. Sohraby, K., Minoli, D., Znati, T. "Wireless sensor networks: technology, protocols, and applications, John Wiley and Sons", 2007
3. Hart, J. K. and Martinez, K. (2006) Environmental Sensor Networks: A revolution in the 4. earth system science? Earth-Science Reviews, 78.
5. Protocols and Architectures for Wireless Sensor Networks Holger Karl, Andreas Willig -08-Oct-2007

MVEP506: LAB I		
Teaching Scheme:	**Examination Scheme(Theory)**	**Examination Scheme (Laboratory)**
Lectures: Nil **Tutorials:** Nil **Practical:** 4Hrs/Week	**TAE:**Nil **CAE :**Nil**ESE:**Nil	**Practical: 100 Marks**
Credit		**2**
Prerequisite (If any):		
Course Objective: 1. To understand software development for embedded systems. 2. To use IDEs for Embedded software development **3.** To understand and implement hardware interfacing with microcontrollers.		
Course Outcome: After successfully completing the course students will be able to		
1. Use software development tools 2. Interface hardware with electronic circuit build with microcontrollers 3. Develop embedded system 4. Development of firmware program for complex system		
List of Assignments The laboratory work will be based on completion of minimum four assignments/experiments confined to the courses of that semester. 1. Modelsim, Xilinx ISE , FPGA/CPLD Board		

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2. To design, prepare layout and simulate CMOS Inverter for the given specifications of load capacitance, propagation delay, power dissipation, foundry etc.
3. To design CMOS logic for F = A + B (C + D) + EFG and prepare layout. Assume suitable capacitive load & foundry. Measure TF,Tf,Tpd
4. Application of Software Development & IDE
   - AVR studio
   - Code Compressor Studio
   - MPLAB
   - UVISION
   - MICROC

7.Develop character device driver for GPIObased on Linux Operating system
8. Write a program for External Interruptbased on Linux Operating system

Scheme of Examination for M.Tech E&TC (VLSI & Embedded System) Course

Branch- E&TC

Semester- II

Subject code	Subject Name	Teaching scheme (Weekly Load in hrs)				Credits	Evaluation Scheme					ESE Duration (Hrs)
							Theory			Practical	Total	
		Lecture	Tutorial	Practical	Total		TAE 20%	CAE 20%	ESE 60%	(Con.Ass.+ External)		
MVEL507	Analog CMOS Design	3	1	_	4	4	20	20	60	_ _	100	
MVEL508	System on Chip	3	1	_	4	4	20	20	60	_ _	100	
MVEL509	Processor Design	3		_	3	3	20	20	60	_ _	100	
MVEL510	Elective II	3	_	_	3	3	20	20	60	_	100	
MVEL511	Elective III	3			3	3	20	20	60		100	
MVEP512	Lab Practice II	_	_	4	4	2	_	_	_	100	100	
MVEP513	Seminar I			2	2	2				100	100	
Total		15	2	6	21	21	100	100	300	200	700	

Elective-III (MVEL511)	Elective -II MVEL510

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MVEL511A. ASIC Design	**MVEL510A**.Microelectronic microwave switches Design(MEMS)
MVEL511B. Network on Chip	
MVEL511C.DSP Processor & Architectures	**MVEL510B**. VLSI Interconnection
MVEL511D. Software Defined Radio	**MVEL510C.** Embedded Product Design
MVEL511E. Energy Studies	**MVEL510D**. Optimization Technique
MVEL511F. Environmental Studies	**MVEL510E**.Design and Analysis of Algorithm
MVEL511G. Open Elective	**MVEL510F**. Industry Offered Elective

MVEL507:ANALOG CMOS DESIGN		
Teaching Scheme:	**Examination Scheme (Theory)**	**Examination Scheme(Laboratory)**
Lectures:3 Hrs/Week **Tutorials:** 1Hr/Week **Practical:**Nil	**TAE:**20 Marks **CAE :**20 Marks**ESE:**60 Marks	**Practical:**Nil
Credit	**4**	
Prerequisite (If any):		
Course Objective:		
1. Knowledge of various MOS based analogcircuits .		
2. Understand design issues related to analog VLSI system.		
3. Understand the working of MOS based data converter circuits		
Course Outcome:		

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1. The student will understand the fundamentals of CMOS Technology in Analog Domain.	
2. The student will show the skills of designing CMOS analog circuits.	
3. The student will demonstrate the ability for using backend tools in analog IC technology.	
Course Contents	**Hrs**
Unit – I :Module I	8
Current sources and References MOSFET as switch, diode and active resistor; MOS Small-signal Models, Common Source Amplifier, The CMOS Inverter as an Amplifier, Weak inversion; Short channel regime; Current sinks and sources; Current mirrors; Current and voltage references, band gap reference.	
Unit – II : Module II	8
CMOS Opamp Inverters, cascade and differential amplifiers; Output amplifier; Opamp, high speed opamp, micro power opamp, low noise opamp.	
Unit – III : Module III	8
Low and High Bandwidth Design Digital to Analog Converters, switched capacitors, Analog to Digital Converters, Bandwidth estimation open and short circuit techniques; Zeros as bandwidth enhancers; Tuned amplifiers.	
Unit – IV : Module IV	8
Low Noise Amplifier Low Noise Amplifier (LNA) design, noise and power trade off, optimizations; Design of mixer; Advanced trends in Radio Frequency (RF) chip design.	

Text Books: (Book Title, Name of the author, name of the Publisher, edition, year of publication)
1. Thomas Lee, “The Design of CMOS Radio – Frequency Integrated Circuits”, Second edition, Cambridge.
2. B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill
Reference Books:
1. Thomas Lee, “The Design of CMOS Radio – Frequency Integrated Circuits”, Second edition, Cambridge.
2. B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill
3. P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, Second Edition, Oxford University Press
4. P. Gray, P. J. Hurst, S. H. Lewis and R. Meyer, *Analysis and Design of Analog Integrated Circuits*, Fourth Edition, Wiley, 2001. (Low Price Edition)

MVEL508: SYSTEM ON CHIP		
Teaching Scheme:	**Examination Scheme(Theory)**	**Examination Scheme (Laboratory)**

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Lectures:3 Hrs/Week **Tutorials:** 1Hr/Week **Practical:**Nil	**TAE:**20 Marks **CAE :**20 Marks**ESE:**60 Marks	**Practical:**Nil
Credit	**4**	

Prerequisite (If any):

Course Objective:

1. This course aims to Model and specify embedded systems at high levels of abstraction.
2. Analyze hardware/software tradeoffs, algorithms, and architectures to optimize the system based on requirements and implementation constraints.
3. Understand hardware, software, and interface synthesis

Course Outcome:

1. The student will learn to design flow graphs and flow modeling.
2. The student will study SOC modeling and interfacing.
3. The student will learn SOC memory system design, embedded software and energy
4. Management techniques for SOC design, SOC prototyping, verification, testing and physical design.
5. The student will able to design , implement and test SOC.

Course Contents	**Hrs**
Unit – I :Module I	8
Basic Concepts: The nature of hardware and software, data flow modeling and implementation,the need for concurrent models, analyzing synchronous data flow graphs, control flow modeling and the limitations of data flow models, software and hardware implementation of data flow, analysis of control flow and data flow, Finite State Machine with data-path, cycle based bit parallel hardware, hardware model , FSMD data-path , simulation and RTL synthesis, language mapping for FSMD.	
Unit – II : Module II	8
Micro-programmed Architectures : limitations of FSM , Micro-programmed : control, encoding , data-path, Micro-programmed machine implementation , handling Micro-program interrupt and pipelining , General purpose embedded cores , processors, The RISC pipeline, program organization, analyzing the quality of compiled code, System on Chip, concept, design principles , portable multimedia system, SOC modeling, hardware/software interfaces , synchronization schemes, memory mapped Interfaces, coprocessor interfaces, coprocessor control shell design, data and control design, Programmer's model .	
Unit – III : Module III	8
RTL intent: Simulation race, simulation-synthesis mismatch, timing analysis, timing parameters for digital logic, factors affecting delay and slew, sequential arcs, clock domain crossing ,bus synchronization , preventing data loss through FIFO, Importance of low power, causes and factors affecting power, switching activity, simulation limitation, implication on synthesis and on backend.	
Unit – IV : Module IV	8

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Research topics in SOC design: A SOC controller for digital still camera, multimedia I P development image and video CODECS, soc memory system design, embedded software, and energy management techniques for SOC design, SOC prototyping, verification, testing and physical design.	

Text Books: (Book Title, Name of the author, name of the Publisher, edition, year of publication)
1. Patrick R. Schaumont, "A Practical Introduction to Hardware/Software Co design", Springer
2. Sanjay Churiwala, SapanGarg , "Principles of VLSI RTL Design A Practical Guide", Springer
Reference Books:
1. Patrick R. Schaumont, "A Practical Introduction to Hardware/Software Co design", Springer
2. Sanjay Churiwala, SapanGarg , "Principles of VLSI RTL Design A Practical Guide", Springer
3. Youn-Long Steve Lin, "Essential Issues in SOC Design, Designing Complex Systems-on-Chip", Springer
4. Wayne Wolf, "Modern VLSI Design Systems on Chip", Pearson Education
5. Rajanish K. Kamat, Santhosh A. Shinde, Vinod G. Shelake, "Unleash the System On Chip using FPGAs and Handel C", Springer

MVEL509: PROCESSOR DESIGN

Teaching Scheme:	**Examination Scheme (Theory)**	**Examination Scheme (Laboratory)**
Lectures:3 Hrs/Week **Tutorials:** Nil **Practical:**Nil	**TAE:**20 Marks **CAE :**20 Marks**ESE:**60 Marks	**Practical:**Nil
Credit	**3**	

Course Outcome:

1. The student will learn Problems, Fallacies and Pitfalls in Processor Design.
2. The student will study Extreme CISC and extreme RISC, Very Long Instruction Word
3. (VLIW), overly aggressive pipelining, unbalanced processor.
4. The student will show skills to implement Processor functional components like MAC.

Course Contents	**Hrs**
Unit – I : Module I	
Embedded Computer Architecture Fundamentals: Components of an embedded computer, Architecture organization, ways of parallelism, I/O operations and peripherals.Problems, Fallacies, and Pitfalls in Processor Design for a high level computer instruction set architecture to support a specific language or language domain, use of intermediate ISAs to allow a simple machine to emulate it"s betters, stack	8

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machines ,overly aggressive pipelining ,unbalanced processor design, Omitting pipeline interlocks, Nonpower-of-2 data-word widths for general-purpose computing	
Unit – II : Module II	8
Memory: Organization, Memory segmentation, Multithreading, Symmetric multiprocessing. **Processor Design flow:** Capturing requirements, Instruction coding, Exploration of architecture organizations, hardware and software development. Extreme CISC and extreme RISC ,Very long instruction word (VLIW),	
Unit – III : Module III	8
Digital signal processor: Digital signal processor and its design issues, evolving architecture of DSP, next generation DSP. **Customizable processors**: Customizable processors and processor customization, A benefit analysis of processor customization, use of microprocessor cores in SOC design, benefits of microprocessor extensibility.	
Unit – IV : Module IV	8
Run time Re-configurable Processors: Run time Re-configurable Processors ,Embedded microprocessor trends, instruction set metamorphosis, reconfigurable computing, run-time reconfigurable instruction set processors ,coarse grain reconfigurable processor. **Processor Clock Generation and Distribution**: Clock parameters and trends, Clock distribution networks, de-skew circuits, jitter reduction techniques, low power clock distribution. **Asynchronous Processor Design**: Asynchronous and self timed processor design, need of asynchronous design, development of asynchronous processors, asynchronous design styles, features of asynchronous design.	

Text Books: (Book Title, Name of the author, name of the Publisher, edition, year of publication)
1. JariNurmi, Processor Design-System on Chip Computing for ASIC‟s and FPGA, Springer Publications.
2. G. Frantz, The DSP and It‟s Impact on the Technology.
Reference Books:
1. JariNurmi, Processor Design-System on Chip Computing for ASIC‟s and FPGA, Springer Publications.
2. G. Frantz, The DSP and It‟s Impact on the Technology.
3. S. Leibson,Tensilica, Customizable Processors and Processor Customization ,
4. F. Campi , Run-Time Reconfigurable Processors

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MVEL510B : VLSI INTERCONNECTIONS		
Teaching Scheme:	**Examination Scheme (Theory)**	**Examination Scheme (Laboratory)**
Lectures:3 Hrs/Week **Tutorials:** Nil **Practical:**Nil	**TAE:**20 Marks **CAE :**20 Marks**ESE:**60 Marks	**Practical:**Nil
Credit	**3**	
Prerequisite (If any):		
Course Objective:		
Course Outcome:		
1. The student will understand the interconnect models.		
2. The student will study delay aspects due to high speed operations.		
3. The student will study futuristic aspects of interconnection		

Course Contents	Hrs
Unit – I : Module I Metal interconnects, Transmission line equations, Analysis of tree structure, Interconnect model based on scattering matrix.	8
Unit – II : Module II Propagation modes, slow wave mode; Parasitic inductances, capacitances, resistances, Ground planes.	8
Unit – III : Module III Propagation modes, slow wave mode; Parasitic inductances, capacitances, resistances, Ground planes, Green‟s function method; Interconnect delays	8
Unit – IV : Module IV Micro strip line model, Analysis, RC models, RLC models; Electromagnetic analysis of multi conductor interconnects; Mesh interconnects, hierarchical interconnects. Switch box routing in PLDs, Optimizations; Future interconnects, Optical interconnects, super conducting interconnects, nano technology circuit interconnects.	8

Text Books: (Book Title, Name of the author, name of the Publisher, edition, year of publication)
1. Ashok K. Goyal, “High Speed VLSI Interconnections”, Second Edition, IEEE Press, John Wiley Publications
2. Michel S. Nakhla, O. J. Zhang, “Modeling and Simulation of High Speed VLSI Interconnects”, Springer Publication
Reference Books:
1. Ashok K. Goyal, “High Speed VLSI Interconnections”, Second Edition, IEEE Press, John Wiley Publications

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2. Michel S. Nakhla, O. J. Zhang, “Modeling and Simulation of High Speed VLSI Interconnects”, Springer Publication

MVEL510C : EMBEDDED PRODUCT DESIGN		
Teaching Scheme:	**Examination Scheme (Theory)**	**Examination Scheme (Laboratory)**
Lectures:3 Hrs/Week **Tutorials:** Nil **Practical:**Nil	**TAE:**20 Marks **CAE :**20 Marks**ESE:**60 Marks	**Practical:**Nil
Credit	**3**	
Prerequisite (If any):		
Course Objective:		
1. To acquaint students with embedded product design process. 2. Identify various models and techniques used for development of hardware and software of embedded system. 3. Identification of Testing ,verification , Certification and documentation process of Embedded Product		
Course Outcome:		
1. The student will study Embedded System & Product specifications, challenges		
2. The student will be able to do cost estimation of Embedded product		
3. The student will understand the aspects of Mechanical Packaging, Testing, reliability and failure analysis, Certification (EMI / RFI) and Documentation		
4. The student will demonstrate the knowledge embedded product design related hardware and software design tools.		

Course Contents	**Hrs**
Unit – I : Module I	8
Overview of embedded products: Need, Design challenges, product survey, specifications of product need of hardware and software, Partitioning of the design into its software and hardware components,Iteration and refinement of the partitioning.	
Unit – II : Module II	8
Deign models and techniques: various models of development of hardware and software, their features, different Processor technology, IC technology, Design Technology.	
Unit – III : Module III	8
Modules of H/W.S/W: Tradeoffs,Custom Single-purpose processors, General-purpose processors, Software, Memory, Interfacing, Design technology-Hardware design, FPGA design, firmware design, driver development, RTOS porting, cost reduction, re-engineering, optimization, maintenance, validation and development, prototyping, turnkey product design.	
Unit – IV : Module IV	8

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Testing and verification: Embedded products-areas of technology, Design and verification, Integration of the hardware and software components, testing- different tools, their selection criterion **Certification and documentation**: Mechanical Packaging, Testing, reliability and failure analysis, communication protocols, Certification (EMI / RFI) and Documentation. Study of any TWO real life embedded products in detail.	

Text Books: (Book Title, Name of the author, name of the Publisher, edition, year of publication)
1. Frank Vahid and Tony Givargis , "Embedded System Design: A Unified Hardware/Software Introduction", John Wiley publication
2. P Marwedel, "Embedded System Design", Springer publication
Reference Books:
1. Frank Vahid and Tony Givargis , "Embedded System Design: A Unified Hardware/Software Introduction", John Wiley publication
2. P Marwedel, "Embedded System Design", Springer publication

MVEL511A: ASIC DESIGN		
Teaching Scheme:	**Examination Scheme (Theory)**	**Examination Scheme (Laboratory)**
Lectures:3 Hrs/Week **Tutorials:** Nil **Practical:**Nil	**TAE:**20 Marks **CAE :**20 Marks**ESE:**60 Marks	**Practical:**Nil
Credit	**3**	
Prerequisite (If any):		
Course Objective:		
1. To prepare the student to be an entry level industrial standard cell ASIC or FPGA designer. 2. To give the student an understanding of issues and tools related to ASIC/FPGA design. 3. Prepare the student for implementation, including timing, performance and power optimization, verification and manufacturing test.		
Course Outcome:		
1. The student will understand the skills of designing analog and digital ASICs.		
2. The student will use the basics of the PLDs for designing IP Cores.		
3. The student will understand the ASIC testing.		
Course Contents		**Hrs**
Unit – I : Module I		8

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Introduction to ASIC : Introduction to ASIC, Types of ASIC, ASIC Design flow, Comparison between ASIC technologies, SIC cell libraries. Design entry by VHDL, Modeling of combinational and sequential circuits, Logic synthesis and logic simulations like static timing analysis, functional simulation and Test benches.	
Unit – II : Module II	8
Mixed Signal ASIC Design **:** Mixed Signal ASIC Design, practical aspects of mix analog digital design, gate level mixed mode simulation, synthesis and testing. A brief introduction to signal integrity effects in ASIC design.	
Unit – III : Module III	8
ASIC construction **:** ASIC construction with goals, objectives and various algorithms for system partitioning, floor-planning placement and routing, Parameter extraction with Post layout simulation and Pre layout simulation.	
Unit – IV : Module IV	8
Testing techniques used in ASIC **:** Testing techniques used in ASIC like Automatic test pattern generation, Scan test, Built in self test and JTAG. Brief view of Stuck at fault models and fault simulation. ASIC Verification and its issues, Types and features of existing available EDA tool.	

Text Books: (Book Title, Name of the author, name of the Publisher, edition, year of publication)
1. Michael Smith, “Application Specific Integrated Circuits” Pearson Education Asia
2. R.S. Soin, F. Maloberti and J. Franca, “Analogue-digital ASICs: circuit techniques, design tools and applications”, IEE Publications
Reference Books:
1. Michael Smith, “Application Specific Integrated Circuits” Pearson Education Asia
2. R.S. Soin, F. Maloberti and J. Franca, “Analogue-digital ASICs: circuit techniques, design tools and applications”, IEE Publications
3. Raminderpal Singh, “Signal Integrity Effects in Custom IC and ASIC Designs”, Wiley Publications

MVEL511B: NETWORK ON CHIP		
Teaching Scheme:	**Examination Scheme (Theory)**	**Examination Scheme (Laboratory)**
Lectures:3 Hrs/Week **Tutorials:** Nil **Practical:**Nil	**TAE:**20 Marks **CAE :**20 Marks**ESE:**60 Marks	**Practical:**Nil
Credit :	**3**	
Prerequisite (If any):		
1. Basics communication		

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Course Objective:	
1. To learn the basic concepts of NOC design by studying the topologies, router design and MPSOC styles,	
2. To learn sample routing algorithms on a NOC with deadlock and live lock avoidance,	
3. To understand the role of system-level design and performance metrics in choosing a NOC design,	
4. To understand the relationship between semiconductor technology, computer architecture and computernetworking in the design of the communication network for a MPSOC or a many-core design.	
Course Outcome:	
1. To learn the basic concepts of NOC design by studying the topologies, router design and MPSOC styles,	
2. To learn sample routing algorithms on a NOC with deadlock and live lock avoidance,	
3. To understand the role of system-level design and performance metrics in choosing a NOC design	
Course Contents	**Hrs**
Unit – I: Communication infrastructure between the many cores of a multi-processor system one-chip (MPSOC)	8
Unit – II Quad-core, eight-core, eighty-core processors that target exa-scale computing or multicore systems that target high-performance mobile computing.	8
Unit – III Systematic understanding, design and analysis of NOCs will be covered.	8
Unit – IV: In particular, the focus will be on topics that include Topology design, Routingalgorithms, Router design	8
Unit – V: Emerging NOC paradigms, System-level performance metrics	8

Text Books: (Book Title, Name of the author, name of the Publisher, edition, year of publication)
1. Architectures A Holistic Design Exploration Chrysostom'sNicopoulos,Vijaykrishnan Narayanan&ChitaR.Das Springer 2001 1st
2. "Networks-on- Chips theory and Practice Fayezgebali,Haythamelmiligi,HqhahedWatheq E1-Kharashi Dramatic Press 2003 2nd
Reference Books:
1. Architectures A Holistic Design Exploration Chrysostom'sNicopoulos,Vijaykrishnan Narayanan&ChitaR.Das Springer 2001 1st
2. "Networks-on- Chips theory and Practice Fayezgebali,Haythamelmiligi,HqhahedWatheq E1-Kharashi Dreamtech Press 2003 2nd
3. Designing Reliable and Efficient Networks on Chips SrinivasanMurali by BPB Publication 2001 1st

MVEL511C: DSP PROCESSORS & ARCHITECTURES		
Teaching Scheme:	**Examination Scheme (Theory)**	**Examination Scheme (Laboratory)**

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Lectures:3 Hrs/Week **Tutorials:** Nil **Practical:**Nil	**TAE:**20 Marks **CAE :**20 Marks**ESE:**60 Marks	**Practical:**Nil
Credit :	**3**	

Prerequisite (If any):

1. Advanced Digital Signal Processing

Course Objective:

1. To impart Digital Signal Processor basics
2. Third generation DSP Architecture and programming skills
3. Advanced DSP architectures and some applications.

Course Outcome:

1. Be able to identify the basic architectural elements of DSP hardware;
2. Understand common real-time DSP algorithms for filtering and multimedia processing applications;
3. Gain an appreciation for the trade-offs necessary in algorithm design for real-time DSP implementation;

Course Contents	**Hrs**
Unit – I : An overview of DSP concepts-Linear system theory, DFT, FFT, realization of digital filters. Typical DSP algorithms, DSP applications.	8
Unit – II : Data flow graph representation of DSP algorithm. Loop bound and iteration bound Retiming and its applications	8
Unit – III : Algorithms for fast convolution. Algorithmic strength reduction in filters and transforms.DCT and inverse DCT. Parallel FIR filters.	8
Unit – IV : Pipelining of FIR filters. Parallel processing. Pipelining and parallel processing for low power. Pipeline interleaving in digital filters. Pipelining and parallel processing for IIR filters. Low power IIR filter design using pipelining and parallel processing, Pipelined adaptive digital filters. Round off noise and its computation.	8
Unit – V : State variable description of digital filters, Round off noise computation using state variable description. Scaling using slow-down, retiming and pipelining	8

Text Books: (Book Title, Name of the author, name of the Publisher, edition, year of publication)

Reference Books:

1. Discrete time signalprocessing Oppenheim and Schaffer Prentice Hall. 1999 1st
2. Digital Signal Processing principals J. G.Proakis, D.G.Manolakis Prentice Hall 2003 1st
3. Theory and Applications of Digital Signal ProcessingRabinar and Gold Prentice Hall 2001 2nd

M ENVLL512D: SOFTWARE DEFINED RADIO

Teaching Scheme:	**Examination Scheme (Theory)**	**Examination Scheme (Laboratory)**

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Lectures:3 Hrs/Week **Tutorials:** Nil **Practical:**Nil	**TAE:**20 Marks **CAE :**20 Marks**ESE:**60 Marks	**Practical:**Nil
Credit	**3**	

Prerequisite (If any):

Course Objective:

1. To enable the student to understand the evolving paradigm of Software Defined radio communication and the enabling technologies for its implementation.
2. To enable the student to understand the essential functionalities and requirements in designing software defined radios and their usage for cognitive communication.
3. To expose the student to the evolving next generation wireless networks and their associated challenges.

Course Outcome:

1. The student will study Needs, Characteristics, Benefits and Design Principles of a Software Radio.
2. The student will be study design aspects of software radios.
3. The student will understand concept of Smart Antennas.
4. The student will study key hardware elements and related Trade-Offs.

Course Contents	Hrs
Unit – I :Module I **Fundamentals of SDR:** Software Radios, Needs, Characteristics, Benefits, Design Principles of a Software Radio, Radio frequency implementation issues, Principal Challenge of Receiver Design	8
Unit – II : Module II **RF and SDR:** RF Receiver Front-End Topologies, Enhanced Flexibility of the RF Chain with Software Radios, Transmitter Architectures and their issues, Noise and Distortion in the RFChain, Timing Recovery in Digital Receivers Using Multirate Digital Filters	8
Unit – III : Module III **Signals in SDR:** Approaches to Direct Digital Synthesis, Analysis of Spurious Signals, Spurious Components due to Periodic Jitter, Band-pass Signal Generation, Hybrid DDS-PLL Systems, Generation of Random Sequences, Parameters of data converters	8
Unit – IV : Module IV **Smart Antennas:** Concept of Smart Antennas, Structures for Beam-forming Systems, Smart Antenna Algorithms, Digital hardware choices, Key Hardware Elements, DSP Processors, Field Programmable Gate Arrays, Trade-Offs in Using DSPs, FPGAs and ASICs **Case studies in Radio System:** Power Management Issues, Object-oriented representation of radios and network resources, Mobile Application Environments, Joint Tactical Radio System, Case studies in software radio design.	8

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Text Books: (Book Title, Name of the author, name of the Publisher, edition, year of publication)
1. Jeffrey H. Reed, “Software Radio: A Modern Approach to Radio Engineering”, Prentice Hall PTR; May 2002 ISBN: 0130811580
2. Dillinger, Madani, Alonistioti (Eds.), “Software Defined Radio, Architectures, Systems and Functions”, Wiley 2003
Reference Books:
1. Jeffrey H. Reed, “Software Radio: A Modern Approach to Radio Engineering”, Prentice Hall PTR; May 2002 ISBN: 0130811580
2. Dillinger, Madani, Alonistioti (Eds.), “Software Defined Radio, Architectures, Systems and Functions”, Wiley 2003
3. Bard, Kovarik, “Software Defined Radio, The Software Communications Architecture”, Wiley 2007
4. Johnson, C.R. and W.A. Sethares, “Telecommunication Breakdown: Concepts of Communication Transmitted via Software-Defined Radio, Pearson Prentice Hall, 2004
5. Bard, John and Kovarik, Vincent, “Software Defined Radio: The Software Communications Architecture”, Wiley Series in Software Radio, 2007

MVEP512: LAB II		
Teaching Scheme:	**Examination Scheme(Theory)**	**Examination Scheme (Laboratory)**
Lectures: Nil **Tutorials:** Nil **Practical:** 4Hrs/Week	**TAE:**Nil **CAE :**Nil**ESE:**Nil	**Practical: 100 Marks**
Credit		**2**
Prerequisite (If any):		
Course Objective: 1. To understand design CMOS circuits . 2. To design, model and interface SoC **3.** To design and implement DSP algorithms on DSP Processor Platform. **4.** To use various EDA Tools for design and simulation		
Course Outcome: After successfully completing the course students		
Use software development tools 1. Should be able to design CMOS circuits 2. Should be able to design, model and interface SoC 3. Should be able to design and implement DSP algorithms on DSP Processor Platform 4. Should be able to use various EDA Tools for design and simulation		

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List of Practical

The laboratory work will be based on completion of minimum four assignments/experiments confined to the courses of that semester.

1. Design, prepare, layout and simulate CMOS Differential Amplifier and Cascade amplifier
2. Design CMOS RF amplifier and suggest suitable technique to enhance BW
3. Design memory system for SoC and Embedded Software and energy management techniques
4. Design adaptive filters using DSP Processor
5. Design a Smart antenna
6. Implement processor functional components like MAC.
7. Writing a VHDL Code to simulate, synthesize, place and route RAM/FIFO on PLD.
8. Draw CMOS layout and simulate full adder/MUX by using DRC appropriate foundry using backend tools and verify outputs

MVEP513: SEMINAR I		
Teaching Scheme:	**Examination Scheme (Theory)**	**Examination Scheme (Laboratory)**
Lectures: Nil **Tutorials:** Nil **Practical:** 2 Hr/Week	**TAE:** Nil **SAE:** Nil **ESE:** Nil	**Marks : 100**
Credit		**2**
Prerequisite (If any):		
Course Objective: Shall be on state of the art topic of students own choice approved by an authority. The student shall submit the duly certified seminar report in standard format, for satisfactory completion of the work by the concerned Guide and head of the department/institute.		

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Scheme of Examination for M. Tech. E & TC Engineering													
VLSI Embedded System Course													
Semester- III													
Subject code	Subject Name	Teaching scheme (Weekly Load in hrs.)				Credits	Evaluation Scheme						ESE Duration (Hrs.)
							Theory			PR		Total	
		Lecture	Tutorial	Practical	Total		TAE 20 %	CAE 20 %	ESE 60%	Internal	External		
MVESD601	Technical Writing (LATEX)	-	-	2	2	2	-	-	-	50	50	100	_
MVEP602	Seminar-II	-	-	4	4	4	-	-	-	50	50	100	-
MVEP603	Dissertation Phase I	-	-	8	8	8	-	-	-	150	50	200	-
	Total	-	-	14	14	14	-	-	-	250	150	400	-

Scheme of Examination for M. Tech. E & TC Engineering													
VLSI Embedded System Course													
Semester-IV													
1	Subject Name	Teaching scheme (Weekly Load in hrs.)				Credits	Evaluation Scheme						ESE Duration (Hrs.)
							Theory			PR		Total	
		Lecture	Tutorial	Practical	Total		TAE 20 %	CAE 20 %	ESE 60%	Internal	External		
MVEP604	Seminar - III	-	-	4	4	4	-	-	-	50	50	100	-
MVEP605	Dissertation Phase II	-	-	16	16	16	-	-	-	150	50	200	-
	Total	-	-	20	20	20	-	-	-	200	100	300	-

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Examination Rules for MTech.

(As per Academic Rule Book July 2016 of GHRCEM)

1. The GradingSystem

Students'performance/ progressshallbeassessedbynumberofcreditshe/shehasearnedsuccessfully. Basedoncoursecreditsandgradepointsobtained bythestudent,semestergradepointaverageand cumulativegradepointaverageshallbecalculated.Theacademicperformanceofastudentshallbe gradedona10-PointScale.Thiscollege shalladopttherelativegrading systeminthelargeracademic interest.

The grading system is produced below:

Grades	Gradepoints	Description
AA	10	Outstanding
AB	9	Excellent
BB	8	Verygood
BC	7	Good
CC	6	Average
CD	5	BelowAverage
DD	4	Marginal
FF	0	Fail

AsperAICTECGPAmaybeconvertedintoequivalentmarksas below:
(CGPA–0.75)x 10=EquivalentPercentage

2.GuidelinesfortheAwardofGrades:

The following are the general guidelines for the award of grades:

i. Foreachstudent,allevaluationsindifferentcomponentsofacourseshallbedoneinabsolute marks considering the weightage in teaching scheme.
ii. Themarksofvariouscomponentsshallbeaddedtogettotalmarkssecuredona10-points scale. The rounding off shall be done on the higher side.
iii. The relative grading systemshall be used for award of grades.
iv. Examination committee shall appoint a sub-committee which shall be called as Grade
v. Moderation committee. (GMC) This committee shall be responsible for grade moderation. Dean academics shall be the convener of Under Graduate programs and PG Head for Post Graduate Programs. Grade shall be awarded by subject teachers and forward it to grade moderation committee through Head of concerned department. Grades shall be modified by the GMC based on the normal distribution.

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2.1 Explanation:'FF Grades

Astudentwhowasawarded“FF”gradeinacorecoursehastorepeatitcompulsorilyfor getting passinggrade isobtained.
Fortheelectivecoursesinwhich'FF'gradehasbeenobtained,thestudentmay takethesame courseoranyothercoursefromthe same category.
Further,'FF' gradessecuredinanycoursestaypermanently onthe gradecard.Theweightageof thesegradesisnotcountedinthecalculation of the CGPA,however these are counted in the calculation of the SGPA.

3.PerformanceIndices

3.1 Grade Point Calculation

1. SGPA will be calculated as per courses registered for the exam in that term and credits earned in the term.
2. SGPA will be Term basis *(Excluding Additional learning courses)*
3. CGPA will be cumulative grade points (∑SGPA *(Excluding Additional learning courses)*) earned till that term.
4. Term Grade points can be calculated for the term *(Excluding Additional learning courses)*

3.2 Calculationof Term GradePointAverage(TGPA)/SemesterGradePointAverage(SGPA)

The performance of a student in a term/semester is indicated by a number called SGPA. The SGPA is the weighted average of the grade points obtained in all the subjects registered by the student during the term/Semester.

$$SGPA = \frac{\sum_{i=1}^{n} C_i P_i}{\sum_{i=1}^{n} C_i}$$

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Where,

Ci=Thenumberofcreditsearnedintheithsubjectofa term/semesterforwhich TGPA/SGPAistobecalculated.
Pi=Gradepointearnedintheithsubject i=1,2,……..,nrepresentthenumberofsubjectsinwhicha studentisregisteredintheconcernedsemester
The TGPA/SGPAiscalculatedtothreedecimalplaces.

3.3 Calculationof CumulativeGradepointAverage(CGPA)

An up-to-date assessment of the overall performance of astudent from the time of his first registrationisobtainedbycalculatinganumbercalledCGPA,which istheweightedaverageof thegradepointsobtainedinallthecoursesin prescribedsemestersfortheUG/PGPrograms. CGPAforastudentofundergraduate/postgraduateProgramsshallbecalculatedonlywhen the grade point (minimum up to pass marks) of all the semester examinations are available.

$$CGPA = \frac{\sum_{j=1}^{m} C_j P_j}{\sum_{j=1}^{m} C_j}$$

Where,Cj=ThenumberofcreditsearnedinthejthsubjectuptothesemesterforwhichCGPA is to be calculated.
Pj =Grade point earned in the jth subject. A grade point less than 4 in a undergraduate subject shallnotbe takenintoconsideration forcalculationofCGPA.Furtheragradepointlessthan 6in a postgraduate subject shall not be taken into consideration for calculationofCGPA
j=1,2,…….,m representthenumberofsubjectsinwhichastudentisregistereduptothe semester for which the CGPA is to be calculated.

The CGPA is also calculated to three decimal places.

4.GradeImprovementScheme PG Program:

ThestudentswhocouldnotgetCGPA6.75willbeallowedtoimprovethegrade from III sem by appearing in maximum two theory subjects in which they got pass grade.

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