



Course wise Teaching Plan for Session : Summer 2019

Course : DIGITAL SYSTEM DESIGN

Faculty : manisha.waje@raisoni.net - MANISHA GOVINDRAO WAJE

| Unit | Topic Code | Topic Covered | Date | Course | Section |
|------|------------|--------------------------------------------------------------------------------------------------------------------------|------------|---------|---------|
| 0 | 1 | Write a VHDL code for different logic gates | 10/12/2018 | BECP204 | A |
| 0 | 1 | Write a VHDL code for different logic gates | 11/12/2018 | BECP204 | A |
| 0 | 1 | Write a VHDL code for different logic gates | 12/12/2018 | BECP204 | A |
| 0 | 1 | Write a VHDL code for different logic gates | 13/12/2018 | BECP204 | A |
| 0 | 2 | Design 4:1 multiplexer and write a VHDL code for same using data flow style of modeling | 17/12/2018 | BECP204 | A |
| 0 | 2 | Design 4:1 multiplexer and write a VHDL code for same using data flow style of modeling | 18/12/2018 | BECP204 | A |
| 0 | 2 | Design 4:1 multiplexer and write a VHDL code for same using data flow style of modeling | 19/12/2018 | BECP204 | A |
| 0 | 2 | Design 4:1 multiplexer and write a VHDL code for same using data flow style of modeling | 20/12/2018 | BECP204 | A |
| 0 | 3 | Design 4-to-16 decoder by combining two 3-to-decoders and write a VHDL code for same using behavioral style of modeling. | 27/12/2018 | BECP204 | A |
| 0 | 3 | Design 4-to-16 decoder by combining two 3-to-decoders and write a VHDL code for same using behavioral style of modeling. | 02/01/2019 | BECP204 | A |
| 0 | 4 | Design BCD to 7 segment decoder and write a VHDL code for same using behavioral style of modeling. | 03/01/2019 | BECP204 | A |
| 0 | 3 | Design 4-to-16 decoder by combining two 3-to-decoders and write a VHDL code for same using behavioral style of modeling. | 07/01/2019 | BECP204 | A |
| 0 | 3 | Design 4-to-16 decoder by combining two 3-to-decoders and write a VHDL code for same using behavioral style of modeling. | 08/01/2019 | BECP204 | A |
| 0 | 4 | Design BCD to 7 segment decoder and write a VHDL code for same using behavioral style of modeling. | 16/01/2019 | BECP204 | A |
| | | | | | |



G H RAISONI COLLEGE OF ENGINEERING AND MANAGEMENT WAGHOLI PUNE

(An Autonomous Institute under UGC Act 1956 & Affiliated to Savitribai Phule Pune University)

Domkhel Road , GAT No.: 1200 Wagholi, Pune – 412207

Course wise Teaching Plan for Session : Summer 2019

Course : DIGITAL SYSTEM DESIGN

Faculty : manisha.waje@raisoni.net - MANISHA GOVINDRAO WAJE

| Unit | Topic Code | Topic Covered | Date | Course | Section |
|------|------------|----------------------------------------------------------------------------------------------------------------|------------|---------|---------|
| 0 | 5 | Design of F/F and write a VHDL code for same using behavioral style of modeling. | 17/01/2019 | BECP204 | A |
| 0 | 4 | Design BCD to 7 segment decoder and write a VHDL code for same using behavioral style of modeling. | 21/01/2019 | BECP204 | A |
| 0 | 4 | Design BCD to 7 segment decoder and write a VHDL code for same using behavioral style of modeling. | 22/01/2019 | BECP204 | A |
| 0 | 5 | Design of F/F and write a VHDL code for same using behavioral style of modeling. | 23/01/2019 | BECP204 | A |
| 0 | 6 | Design half adder and full adder and write a VHDL code for same using dataflow style of modeling.. | 24/01/2019 | BECP204 | A |
| 0 | 5 | Design of F/F and write a VHDL code for same using behavioral style of modeling. | 28/01/2019 | BECP204 | A |
| 0 | 5 | Design of F/F and write a VHDL code for same using behavioral style of modeling. | 29/01/2019 | BECP204 | A |
| 0 | 6 | Design half adder and full adder and write a VHDL code for same using dataflow style of modeling.. | 04/02/2019 | BECP204 | A |
| 0 | 6 | Design half adder and full adder and write a VHDL code for same using dataflow style of modeling.. | 05/02/2019 | BECP204 | A |
| 0 | 6 | Design half adder and full adder and write a VHDL code for same using dataflow style of modeling.. | 06/02/2019 | BECP204 | A |
| 0 | 7 | Design a 9-bit Parity generator circuit and write a VHDL code for the same using structural style of modeling. | 07/02/2019 | BECP204 | A |
| 0 | 7 | Design a 9-bit Parity generator circuit and write a VHDL code for the same using structural style of modeling. | 11/02/2019 | BECP204 | A |
| 0 | 7 | Design a 9-bit Parity generator circuit and write a VHDL code for the same using structural style of modeling. | 12/02/2019 | BECP204 | A |
| 0 | 7 | Design a 9-bit Parity generator circuit and write a VHDL code for the same using structural style of modeling. | 13/02/2019 | BECP204 | A |
| | | | | | |

**Course wise Teaching Plan for Session : Summer 2019****Course : DIGITAL SYSTEM DESIGN****Faculty : manisha.waje@raisoni.net - MANISHA GOVINDRAO WAJE**

| Unit | Topic Code | Topic Covered | Date | Course | Section |
|-------------|-------------------|-----------------------------------------------------------------------------------------------------------------|-------------|---------------|----------------|
| 0 | 8 | Design of Finite state machine to detect a sequence "1011" using Mealy model .and write VHDL code for the same. | 14/02/2019 | BECP204 | A |
| 0 | 8 | Design of Finite state machine to detect a sequence "1011" using Mealy model .and write VHDL code for the same. | 25/02/2019 | BECP204 | A |
| 0 | 8 | Design of Finite state machine to detect a sequence "1011" using Mealy model .and write VHDL code for the same. | 26/02/2019 | BECP204 | A |
| 0 | 8 | Design of Finite state machine to detect a sequence "1011" using Mealy model .and write VHDL code for the same. | 27/02/2019 | BECP204 | A |
| 0 | 9 | Design 16:1 MUX using 4:1 MUX using structural style of modeling. | 28/02/2019 | BECP204 | A |
| 0 | 9 | Design 16:1 MUX using 4:1 MUX using structural style of modeling. | 04/03/2019 | BECP204 | A |
| 0 | 9 | Design 16:1 MUX using 4:1 MUX using structural style of modeling. | 05/03/2019 | BECP204 | A |
| 0 | 9 | Design 16:1 MUX using 4:1 MUX using structural style of modeling. | 06/03/2019 | BECP204 | A |
| 0 | 10 | Design Arithmetic and Logic Unit. | 07/03/2019 | BECP204 | A |
| 0 | 10 | Design Arithmetic and Logic Unit. | 18/03/2019 | BECP204 | A |
| 0 | 10 | Design Arithmetic and Logic Unit. | 19/03/2019 | BECP204 | A |
| 0 | 10 | Design Arithmetic and Logic Unit. | 20/03/2019 | BECP204 | A |