Course wise TeachingPlan for Session : Summer 2019

Course : DIGITAL SYSTEM DESIGN **Faculty : manisha.waje@raisoni.net - MANISHA GOVINDRAO WAJE**

Unit	Topic Code	Topic Covered	Date	Course	Section
1	1	Syllabus Discussion, Discussion on course objective & course outcome, Basic Terminology, Design Units, Identifiers, Entity Declaration , Architecture Body , Data Objects, Data Types, VHDL Operators, Attributes, VHDL Modelling Styles	07/12/2018	BECL204	A
1	2	Modelling Styles: Data flow with Examples	14/12/2018	BECL204	A
1	3	Modelling Styles: Behavioral with Examples	21/12/2018	BECL204	A
1	4	Modelling Styles: Structural with Examples	28/12/2018	BECL204	A
2	5	Concurrent signal assignment statements, Sequential Signal assignment statements with example	04/01/2019	BECL204	A
2	6	Wait statement, IF statement, Case statement, Null statement, Exit statement, Next statement, Process statement, Examples on Conditional signal assignment, Conditional signal assignment	18/01/2019	BECL204	A
3	7	Package body and Package declaration with example, Inertial delay, Transport delay, Delta delay, Signal Drivers	25/01/2019	BECL204	A
3	8	test bench, component declaration, instantiation, Examples on Test Bench, Generate statement, generic statement with examples	01/02/2019	BECL204	A
4	9	Combinational logic circuit design and VHDL implementation of following circuits –Adders, Subtractors, Multiplexers, Encoders, Decoders,	08/02/2019	BECL204	A
4	10	Combinational logic circuit design and VHDL implementation of following circuits - BCD to 7segment decoder, 4-bit adder, comparator, Arithmetic Logic Unit	15/02/2019	BECL204	A
5	11	Sequential logic circuit design and VHDL implementation of following circuits: flip-flops, Latches, Registers , Counters, Mealy , Moore	22/02/2019	BECL204	A
6	12	Examples on ROM, PLA, PAL Architecture of FPGA(Xilinx / Altera),	01/03/2019	BECL204	A

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Unit	Topic Code	Topic Covered	Date	Course	Section
6	13	Introduction to place & route process	08/03/2019	BECL204	A